A binary counter is constructed with flip-flops and it takes the outputs of one cell and moves it to the clock input of the next. In VHDL, to convert from integer to std\_logic\_vector you use the to\_signed() function. When you convert from std\_logic\_vector to integer, you use the signed() typecast. The block diagram for the 8-bit counter made of 2 4-bit counters is below:

Graphical user interface

Description automatically generated with medium confidence